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10/021,009	12/19/2001	Hong Sung Song	041501-5686	8778
9629 7590 07/09/2010 MORGAN LEWIS & BOCKIUS LLP 1111 PENNSYLVANIA AVENUE NW WASHINGTON, DC 20004				
EXAMINER				
BODDIE, WILLIAM				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/021,009

Applicant(s)

SONG, HONG SUNG

Examiner

WILLIAM L. BODDIE

Art Unit

2629

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-5,8-10,12 and 13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5,8-10,12 and 13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB-06)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. In an amendment dated, June 23rd, 2010, the Applicant amended claims 1, 5 and 10. Currently claims 1, 3-5, 8-10 and 12-13 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 3-5, 8-10 and 12-13 have been considered but they are unpersuasive.
3. On page 9 of the Remarks, the Applicants argue that Wada fails to teach supplying the DOE signal to a first and second delay means and that the DOE signal is sued to make the data driving circuit apply the data to the data lines.
4. The Examiner respectfully disagrees. The 70-7 signal of Wada is clearly supplied to a first and second flip flop labeled as 10 in figure 2. Furthermore, it is the Examiner's understanding that the output signal generated by the 10-12 elements in figure 2 of Wada is a display prohibiting signal. This display prohibiting signal is then supplied to the driving signal creation circuit (8 in fig. 2) stopping the driving signal creation. With this manner of operation, it seems clear to the Examiner, that the 70-7 clock signal input to the delay means directly results in the production of a display prohibiting signal. This display prohibiting signal performs the function to enable and disable driving signal creation thereby directly affecting the data driving integrated circuit. To further explain, the 70-7 clock signal is seen as directly affecting the data driving integrated circuit. The clock signal is an input to a circuit which generates an output signal that turns on/off the supply of driving signals. Without driving signals the application of data via the data driving integrated circuit is impossible. As shown above,

it is the Examiner's belief that the 70-7 delay clock of Wada fulfills the broadest reasonable interpretation of the limitation requiring that the signal result in the application of data to data lines by the data driving integrated circuit.

5. Applicant's arguments on pages 10-11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 3-5, 8-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,648,793) in view of Yamazaki (US 6,522,319) and Wada et al. (JP 01-106,017) and further in view of Asada et al. (US 5,867,141).

With respect to claim 1, Chen discloses, a method of driving a liquid crystal display panel of a dot inversion system (fig. 4(c); col. 3, lines 63-65) having liquid crystal cells (p11-p44 in fig. 1a) arranged at intersections between a plurality of data lines (D1-D4 in fig. 1a) and a plurality of gate lines (G1-G4 in fig. 1a) in a matrix array, comprising the steps of:

supplying the data lines with (n-2)th data (D1 value at T3 in fig. 5) corresponding to the liquid crystal cells connected to an (n-2)th gate line (G1 in fig. 5), wherein n is an integer greater than 2;

conducting a first data supplying channel (note the selection pulse on G3 at T3 in fig. 5) for the liquid crystal cells connected to the nth gate line (G3 in fig. 5) such that the (n-2)th data is supplied to the liquid crystal cells connected to the nth gate line;

conducting a second data supplying channel for the liquid crystal cells connected to the (n-2)th gate line (G1 in fig. 5) such that the (n-2)th data is supplied to the liquid crystal cells connected to the (n-2)th gate line (note the voltage of pixel P11 in fig. 5),

wherein conducting the first data supplying channel and conducting the second data supplying channel are performed substantially simultaneously (both G1 and G3 are driven simultaneously at T3 in fig. 5; col. 3, lines 45-47),

wherein the liquid crystal cells connected to only first and second gate lines of the plurality of gate lines are supplied with active data signals (T3 for G1 and T4 for G2 in fig. 5) after precharging (col. 3, lines 39-45 and col. 4, lines 26-31; all of the other cells are supplied with active data signals in the previous frame; prior to the first and second row cells);

wherein a time at which the data is applied to the liquid crystal cell is greater than a switching time required for applying the data to the liquid crystal cell (see the waveform on P21 in fig. 5, during its data signal application (T4 in fig. 5); seems clear from the waveform the switching time requires less time than the application of data to the liquid crystal cell).

Chen does not expressly disclose, supplying gate start pulses to conduct data supplying channels, or that the first and second gate start pulses are output from a pre-charging controller.

Yamazaki discloses, supplying gate start pulses (output of drive voltage forming circuit) to a gate driver (2 in fig. 1), that in response generate pulses on gate electrodes (fig. 3; for example), and that the first and second gate start pulses are output from a pre-charging controller (4 in fig. 1);

wherein the pre-charging controller is supplied with a data output enable signal (LP in fig. 1) for controlling data output of a data driving integrated circuit (3 in fig. 1), wherein the data driving integrated circuit applies data to the data lines in response to the data output enable signal (col. 28, line 65 – col. 29, line 8), and wherein the data output enable signal is directly applied to the data driving integrated circuit and the pre-charging controller (LP if directly applied to both 4 and 3 in fig. 1).

Chen and Yamazaki are analogous art because they are both from the same field of endeavor namely, LCD panel gate driving methods and circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the gate start pulses, taught by Yamazaki, to generate the gate electrode pulses of the LCD panel of Chen.

The motivation for doing so would have been to above direct-current application and crosstalk (Yamazaki col. 12, lines 5-18).

Neither Yamazaki nor Chen expressly disclose that the inner circuitry of the precharging controller.

Wada discloses, LCD drive circuitry (line 2-3 of constitution) to generate a select signal (b in fig. 2) that includes pre-charging controller circuitry including:

a first input line (D in the left flip-flop 10 in fig. 2) supplied with a pre-gate start pulse (FR in fig. 2) and a second input line (CK in left flip-flop 10 in fig. 2) supplied with a data output enable signal (DOE) (70-7 in fig. 2) for controlling data output of a data driving integrated circuit (constitution), wherein the data driving integrated circuit applies data to the data lines in response to the data output enable signal (70-7 is also applied to a polarity switching circuit, 9 in fig. 2, which in turn controls the driving signal generating circuit 8 in fig. 2; thus the 70-7 signal of Wada is directly responsible for the polarity of the signal that is output to the data lines);

first delay means (10; left D flip-flop in fig. 2) for delaying the pre-gate start pulse from the first input line by one clock interval of the data output enable signal in response to the data output enable signal (as Wada's circuitry is identical to Applicant's this operation will be inherent);

second delay means (10; right D flip-flop in fig. 2) for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data output enable signal in response to data output enable signal (as Wada's circuitry is identical to Applicant's this operation will be inherent); and

a gate device for executing an exclusive logical sum operation (11 in fig. 2) of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses (constitution).

Wada, Chen and Yamazaki are analogous art because they are all from the same field of endeavor namely, LCD panel gate driving methods and circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the precharging controller of Yamazaki and Chen with the delay means and gates taught by Wada.

The motivation for doing so would have been to eliminate irregularity in cost (Wada; purpose).

Chen further discloses precharging the first and second gate lines at every frame with data signals (T1, T2 in fig. 5; col. 3, lines 39-45).

Neither Chen, Wada nor Yamazaki expressly disclose that the first and second gate lines are precharged during a blanking interval.

Asada discloses only the first and second gate lines are charged in advance with data signal at every frame with data signal applied at a blanking interval (abstract and col. 5, lines 18-38; all the other cells are charged after they have been supplied an active data signal).

Chen, Wada, Yamazaki and Asada are analogous art because they are both from the same field of endeavor namely, gate driving methods of liquid crystal displays.

At the time of the invention it would have been obvious to one of ordinary skill in the art to drive the LCD of Chen, Wada and Yamazaki during T1-T2 as a blanking interval, as taught by Asada.

The motivation for doing so would have been to generate images with competent image quality and a stable high contrast (Asada; col. 3, lines 64-65).

With respect to claim 3, Chen, Wada, Yamazaki and Asada disclose, the method according to claim 1 (see above).

Chen further discloses, wherein polarity inversion of the data signals (D1 in fig. 5) applied to the liquid crystal cells connected to the first and second gate lines (G1, G2 in fig. 5) is made in at least two clock time intervals prior to an application of an active data signal (T3 for G1 and T4 for G2) (the pre-charge data must undergo polarity inversion prior to be applied (prior to T1 for G1), this is clearly two clock intervals prior to the application of the active data signal (T3 for G1); also note col. 3, lines 39-45 and col. 4, lines 26-31).

With respect to claim 4, Chen, Wada, Yamazaki and Asada disclose, the method according to claim 1 (see above).

Chen further discloses, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines (G1 and G2 in fig. 5) are applied in at least two clock time intervals before the gate and data control signals become effective data (fig. 5; Chen delays the control signals applied to the first and second gate lines; and also discloses different lengths of driving pulses; col. 3, lines 42-45; col. 4, lines 26-31).

With respect to claim 5, Chen discloses, a driving apparatus for a liquid crystal display panel of a dot inversion system (fig. 4(c); col. 3, lines 63-65) having liquid crystal cells (p11-p44 in fig. 1a) arranged at intersections between a plurality of data lines (D1-D4 in fig. 1a) and a plurality of sequentially driven gate lines (G1-G4 in fig. 1a; fig. 5) in a matrix array comprising:

continuously generating first and second gate pulses (pulses on G3 and G1 for example, col. 4, lines 26-31) to supply an (n-2)th data corresponding to liquid crystal

cells connected to an $(n-2)$ th gate line to both liquid crystal cells connected to an n th gate line and liquid crystal cells connected to the $(n-2)$ th gate line, wherein n is an integer greater than 2 (fig. 5; col. 3, lines 45-47),

wherein the liquid crystal cells connected to only first and second gate lines of the plurality of gate lines are supplied with active data signal (T3 for G1 and T4 for G2 in fig. 5) after precharging (col. 3, lines 39-45 and col. 4, lines 26-31; all of the other cells are supplied with active data signals in the previous frame; prior to the first and second row cells);

wherein a time at which the data is applied to the liquid crystal cell is greater than a switching time required for applying the data to the liquid crystal cell (see the waveform on P21 in fig. 5, during its data signal application (T4 in fig. 5); seems clear from the waveform the switching time requires less time than the application of data to the liquid crystal cell).

Chen does not expressly disclose, a data/gate driving integrated circuit or a pre-charging controller that includes an XOR gate.

Yamazaki discloses, a data driving integrated circuit supplying data to the data lines of the liquid crystal display panel (3 in fig. 1);

a gate driving integrated circuit (2 in fig. 1) responsive to first and second gate start pulses (VH, VL in fig. 2) to drive the gate lines of the liquid crystal display panel (fig. 3); and

a pre-charging controller (4 in fig. 1) to generate the first and second gate start pulses (clear from fig. 2, that the device generates the VH and VL voltage pulses that are applied to the Y driver in fig. 1);

wherein the pre-charging controller is supplied with a data output enable signal (LP in fig. 1) for controlling data output of a data driving integrated circuit (3 in fig. 1), and wherein the data driving integrated circuit applies data to the data lines in response to the data output enable signal (col. 28, line 65 – col. 29, line 8); and

wherein the data output enable signal is directly applied to the data driving integrated circuit and the pre-charging controller (LP if directly applied to both 4 and 3 in fig. 1).

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the gate start pulses, taught by Yamazaki, to generate the gate electrode pulses of the LCD panel of Chen.

The motivation for doing so would have been to above direct-current application and crosstalk (Yamazaki; col. 12, lines 5-18).

Neither Yamazaki nor Chen expressly disclose that the inner circuitry of the precharging controller.

Wada discloses, LCD drive circuitry (line 2-3 of constitution) to generate a select signal (b in fig. 2) that includes pre-charging controller circuitry including:

a first input line (D in the left flip-flop 10 in fig. 2) supplied with a pre-gate start pulse (FR in fig. 2) and a second input line (CK in left flip-flop 10 in fig. 2) supplied with a data output enable signal (70-7 in fig. 2) for controlling data output of a data driving

integrated circuit (constitution), wherein the data driving integrated circuit applies data to the data lines in response to the data output enable signal (DOE) (70-7 is also applied to a polarity switching circuit, 9 in fig. 2, which in turn controls the driving signal generating circuit 8 in fig. 2; thus the 70-7 signal of Wada is directly responsible for the polarity of the signal that is output to the data lines);

first delay means (10; left D flip-flop in fig. 2) for delaying the pre-gate start pulse from the first input line by one clock interval of the data output enable signal in response to the data output enable signal (as Wada's circuitry is identical to Applicant's this operation will be inherent);

second delay means (10; right D flip-flop in fig. 2) for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data output enable signal in response to a data output enable signal (as Wada's circuitry is identical to Applicant's this operation will be inherent); and

a gate device for executing an exclusive logical sum operation (11 in fig. 2) of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses (constitution).

At the time of the invention it would have been obvious to one of ordinary skill in the art to construct the precharging controller of Yamazaki and Chen with the delay means and gates taught by Wada.

The motivation for doing so would have been to eliminate irregularity in cost (Wada; purpose).

Neither Chen, Wada nor Yamazaki expressly disclose that the first and second gate lines are precharged during a blanking interval.

Asada discloses only the first and second gate lines are charged in advance with data signal at every frame with data signal applied at a blanking interval (abstract and col. 5, lines 18-38; all the other cells are charged after they have been supplied an active data signal).

At the time of the invention it would have been obvious to one of ordinary skill in the art to drive the LCD of Chen, Wada and Yamazaki during T1-T2 as a blanking interval, as taught by Asada.

The motivation for doing so would have been to generate images with competent image quality and a stable high contrast (Asada; col. 3, lines 64-65).

With respect to claim 8-9, Chen, Wada, Yamazaki and Asada disclose, the apparatus according to claim 5 (see above).

As claims 8-9 are identical limitations to those recited in claims 3-4 they are rejected on the same merits shown above.

With respect to claim 10, currently it appears that claim 10 is merely a broader version of claim 5, as it is exempt from the limitations of sequential gate driving and use of the dot inversion system. Therefore claim 10 is rejected based on the same merits shown above in the rejection of claim 5.

With respect to claim 12, Chen, Wada, Yamazaki and Asada disclose, the method according to claim 10 (see above).

Chen further discloses, wherein polarity inversion of the data signals (D1 in fig. 5) applied to the liquid crystal cells connected to the first and second gate lines (G1, G2 in fig. 5) is made in at least two clock time intervals prior to an application of an active data signal (T3 for G1 and T4 for G2) (the pre-charge data must undergo polarity inversion prior to be applied (prior to T1 for G1), this is clearly two clock intervals prior to the application of active data (T3 for G1); also note col. 3, lines 39-45 and col. 4, lines 26-31).

With respect to claim 13, Chen, Wada, Yamazaki and Asada disclose, the method according to claim 10 (see above).

Chen further discloses, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines (G1 and G2 in fig. 5) are applied in at least two clock time intervals before the gate and data control signals become effective data (fig. 5; Chen delays the control signals applied to the first and second gate lines; and also discloses different lengths of driving pulses; col. 3, lines 42-45; col. 4, lines 26-31).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM L. BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/William L Boddie/
Examiner, Art Unit 2629
7/9/10